REMARKS

Summary of Claim Status

Claims 1-21 and 23-25 are pending in the present application after entry of the present amendment, and are rejected for the reasons discussed below. Applicants have canceled Claim 22, thereby rendering its rejection moot. Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections in view of the present amendment and in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 1-25 are rejected under 35 U.S.C. § 102(b) as being anticipated by Calderone et al., U.S. Patent No. 6,507,942 ("Calderone"). Applicants respectfully traverse the rejection with respect to all claims.

Applicants have amended Claim 1 to recite:

> wherein if the at least one underperforming region is layout sensitive, the step of adjusting comprises adjusting the layout of the at least one of the plurality of configurable devices; and
>
> wherein if the at least one underperforming region is not layout sensitive, the step of adjusting comprises adjusting the fabrication process.

Applicants respectfully submit that Calderone does not teach or even suggest the invention recited in Claim 1, as amended. In particular, Calderone does not teach determining if an underperforming region is layout sensitive, and does not teach adjusting the layout if the underperforming region is layout sensitive. In fact, nowhere in Calderone are determining layout sensitivity and adjusting a layout even mentioned, much less taught or disclosed.

Calderone is generally directed to systems and methods for measuring uniformity of a fabrication process. See, e.g., Calderone at Abstract. Fig. 5 of Calderone shows a step 535 of adjusting an IC-process mask sequence, where "the process sequence used to form the IC is analyzed and adjusted as necessary to improve critical-dimension uniformity." Calderone at col. 4, lines 20-24. Thus, Calderone deals with testing a fabrication process, and making adjustments to the

fabrication process to ensure uniformity. More specifically, there is no mention of determining layout sensitivity since Calderone is focused on improving uniformity of a fabrication process.

In contrast, Claim 1 recites steps of determining if an underperforming region is layout sensitive, and adjusting the layout if the underperforming region is layout sensitive. Calderone does not teach or even suggest such features. In fact, the word "layout" is never even mentioned in Calderone, and thus it would be impossible for Calderone to teach the invention of Claim 1. Instead, Calderone appears to be concerned with testing and improving uniformity in a fabrication process. Therefore, Applicants believe Claim 1 is allowable, and allowance of Claim 1 is respectfully requested.

Claims 2-20 depend, either directly or indirectly, from Claim 1, and thus include all of the limitations of Claim 1. For at least the reasons set forth above, Applicants believe Claim 1 is allowable. Therefore, for at least the same reasons, Applicants believe Claims 2-20 are also allowable, and allowance of such claims is respectfully requested.

Applicants have amended Claim 21 to include the features of canceled Claim 22. Applicants believe Calderone does not teach or even suggest the features of Claim 21. In particular, Claim 21 recites a wafer comprising a plurality of configurable devices, a tester coupled to the wafer, and a probe card coupled between the tester and the wafer. Applicants respectfully submit that Calderone does not teach or disclose at least these features.

First, Calderone does not even mention the word "wafer," much less teach or disclose a wafer comprising a plurality of configurable devices. As shown in Fig. 6 of Calderone, the IC 610 being tested is diced from the wafer, packaged, and placed on a conventional PC board 605. The PC board 605 may then be connects to a processor 612 such as a computer, which is adapted to measure the speed performance of IC 610. Thus, the IC being tested in Calderone is removed from the wafer.

Furthermore, Calderone does not teach or even mention a probe card. As shown in Fig. 6 of Calderone, the IC 610 being tested is coupled to a processor 612 through a board 605 and a bus 608. In particular, there is no probe card, which is generally used with unpackaged device such as devices still attached to a wafer, coupled between the processor and the IC in Calderone.

In contrast, the invention recited in Claim 21 includes a wafer comprising a plurality of configurable devices and a probe card coupled between a tester and the wafer. As shown in the examples of Figs. 2 and 4A-C, testing the wafers advantageously allows for determining whether an underperforming region is layout sensitive. Applicants respectfully submit that Calderone does not teach or even suggest the invention recited in Claim 21. Therefore, Applicants respectfully request allowance of Claim 21.

Claims 23 and 24 depend, either directly or indirectly, from Claim 21, and thus include all of the limitations of Claim 21. For at least the reasons set forth above, Applicants believe Claim 21 is allowable. Therefore, for at least the same reasons, Applicants believe Claims 23 and 24 are also allowable, and allowance of such claims is respectfully requested.

Applicants have amended Claim 25 in a manner similar to the amendment of Claim 1. In particular, Claim 25 recites if the at least one underperforming region is layout sensitive, the means for adjusting adjusts the layout of the at least one of the plurality of configurable devices, and if the at least one underperforming region is not layout sensitive, the means for adjusting adjusts the fabrication process. As set forth above with respect to Claim 1, Calderone does not teach or suggest determining if an underperforming region is layout sensitive, and does not teach or suggest adjusting a layout. Therefore, Applicants believe Claim 25 is allowable over Calderone, and allowance of Claim 25 is respectfully requested.

All of the above amendments are fully supported by the specification, for example in Figure 2 and the corresponding text.

CONCLUSION

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicants believe that Claims 1-21 and 23-25 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on September 9, 2005.

Julie Matthews
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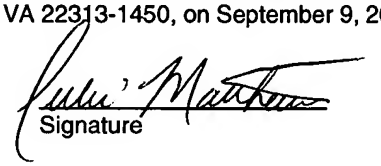

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